

- Wire D0, D1 to Ucc, D2 to ground (don't connect anything to D0&D1 - pullup resistors active, insert J1)
- Send a pulse to FQ_UD

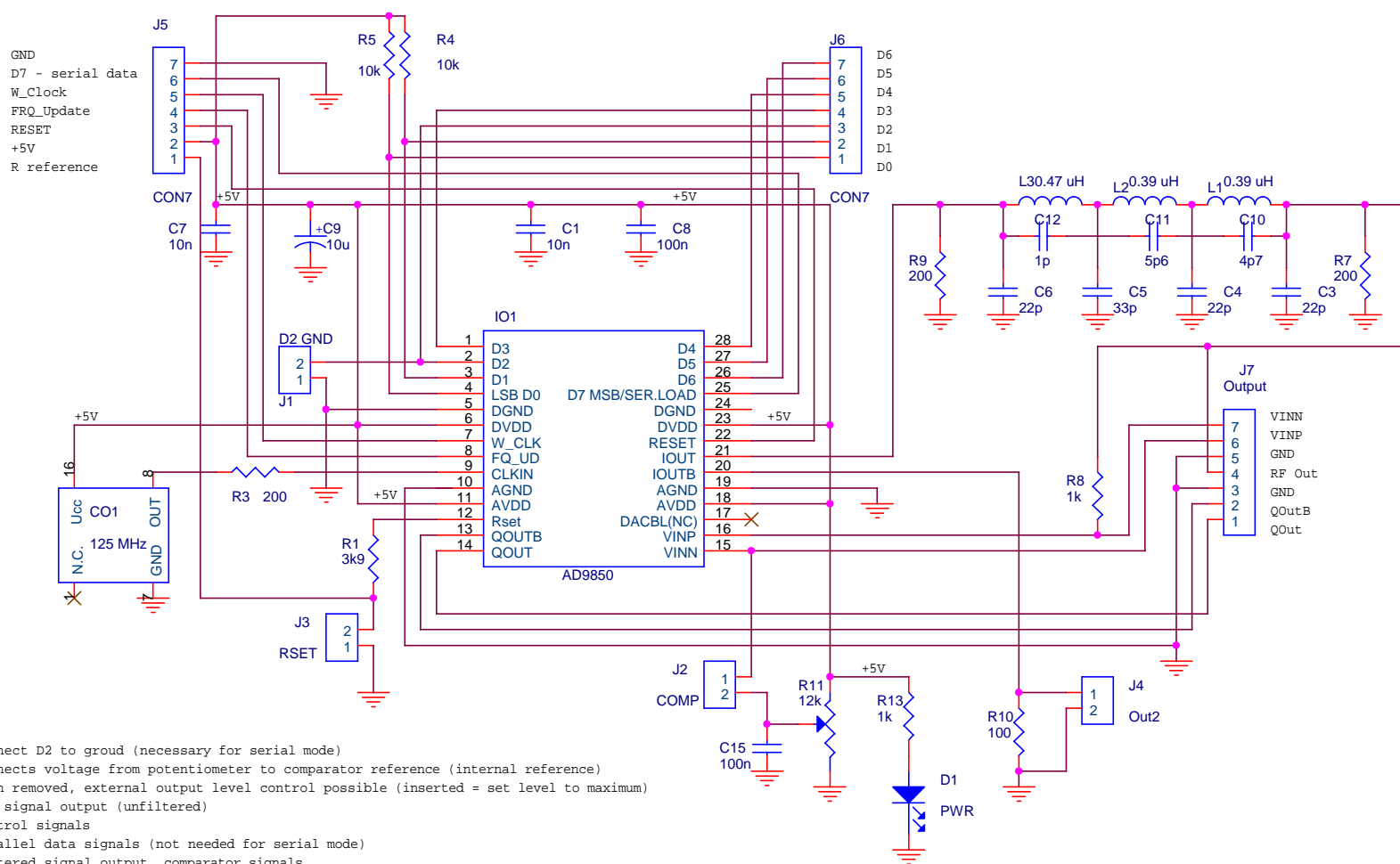
Signals:

FR_UP - rising edge updates the freq, resets data transfer pointer

W CLK - serial data clock. Data signal must be valid while W CLK is active.

D7 - serial data pin. Sequence consists of 40 bits (32 freq, 5 phase, 3 control bits)

RESET - high performs reset. Connect to ground for normal operation.



Jumpers:

- J1 - connect D2 to ground (necessary for serial mode)
- J2 - connects voltage from potentiometer to comparator reference (internal reference)
- J3 - when removed, external output level control possible (inserted = set level to maximum)
- J4 - 2nd signal output (unfiltered)
- J5 - control signals
- J6 - parallel data signals (not needed for serial mode)
- J7 - filtered signal output, comparator signals

Working with controller board:

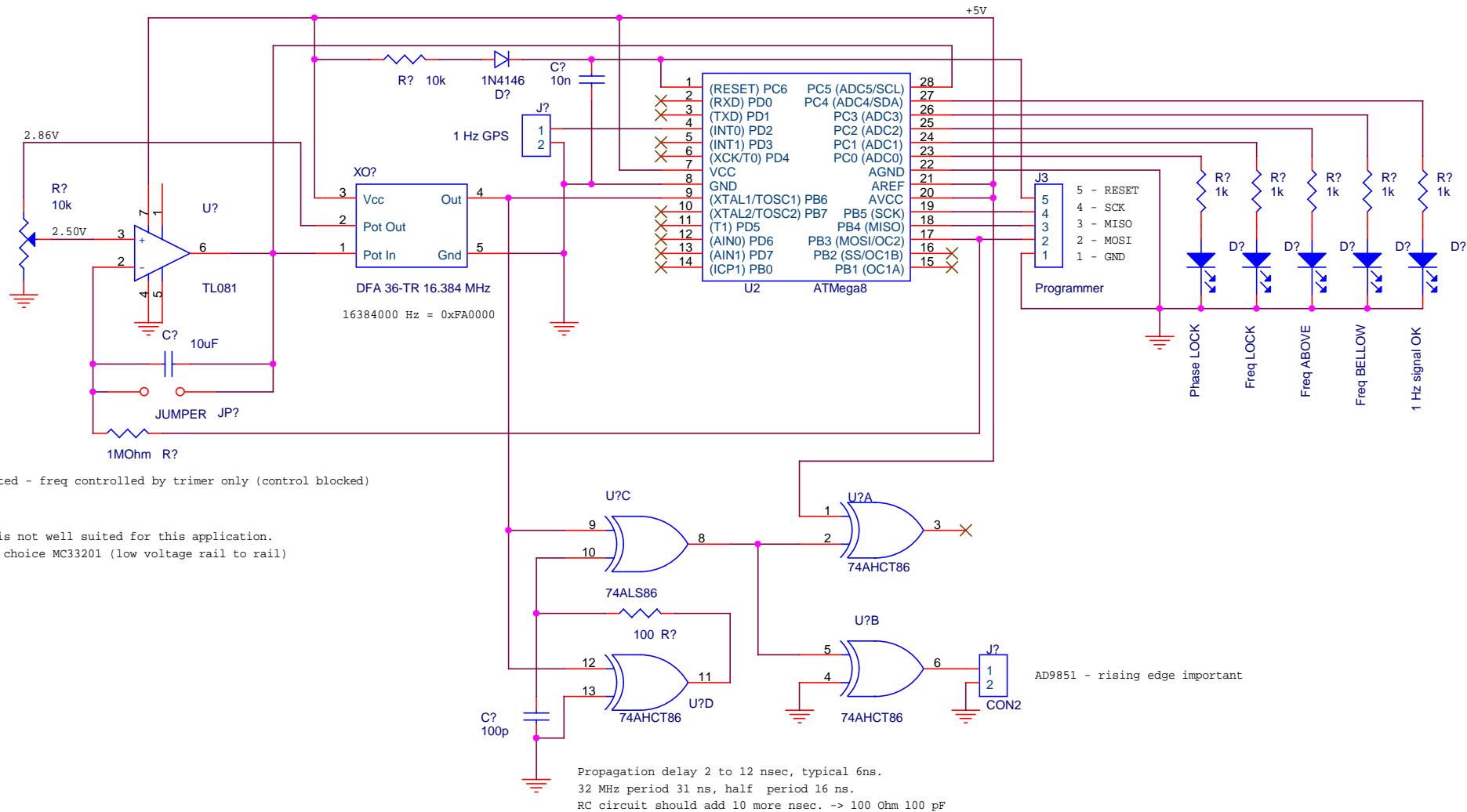
- J1 jumper not necessary (connected to GND on processor board)
 J2 jumper inserted (comparator not used, VINP connected to GND on controller board, but...)
 J3 jumper not necessary (connected to GND on processor board)
 J4 output not used, spare
 J6 all pins grounded on controller board

Compiled from original chinese circuit diagram and own measurement (there are differencies!)

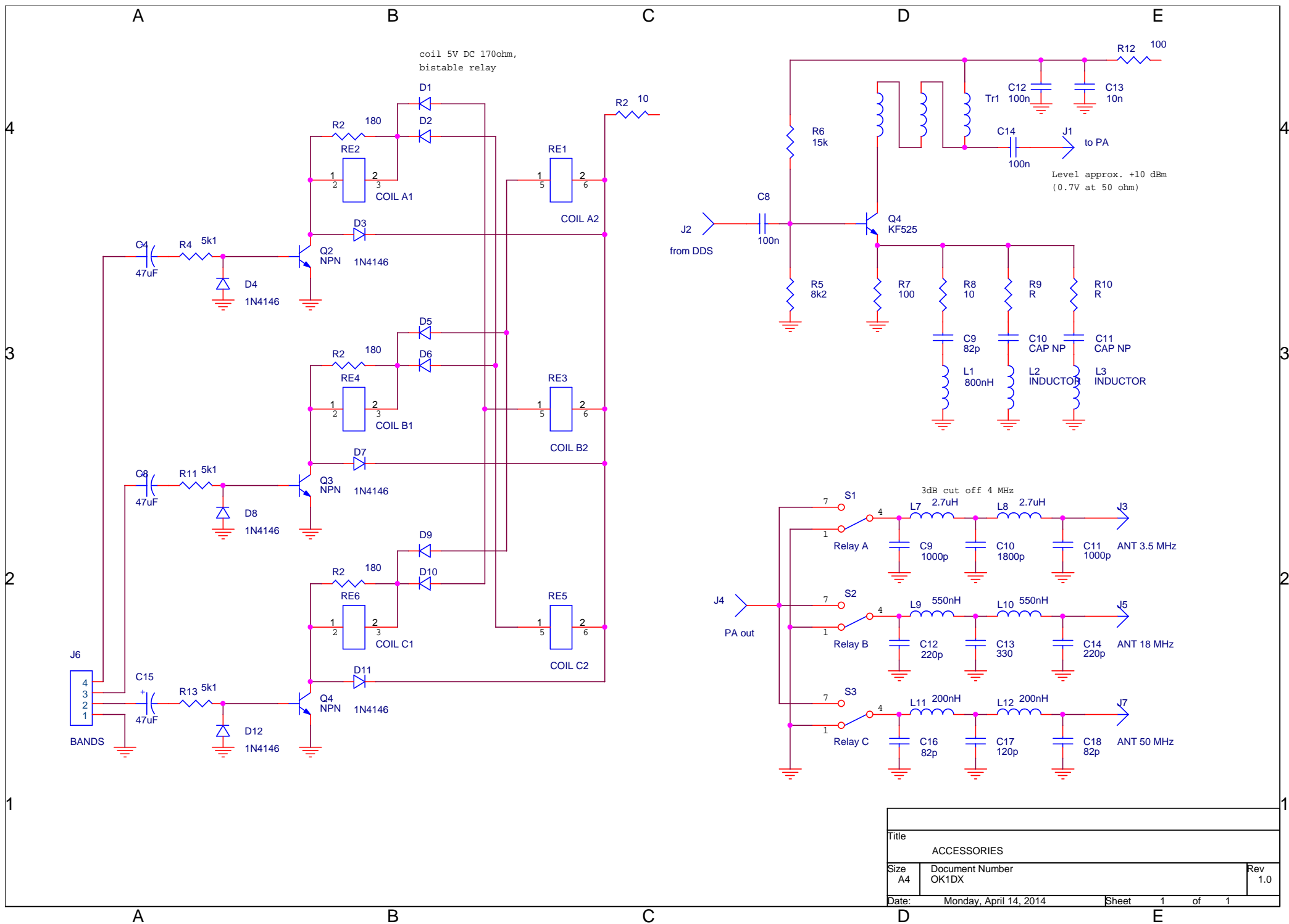
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Pot Out - internal 4V stabilizer with 4 kOhm in series (loaded by 10 kOhm potentiometer -> 2.86V)
 Pot In - 30 microA by 4V signal (about 100 kOhm)
 Vcc - TCXO works between 3 and 7 V (or more?)
 Out - TTL square voltage, level not changing for Vcc > 4V

External clock - fuses CKSEL 0000



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