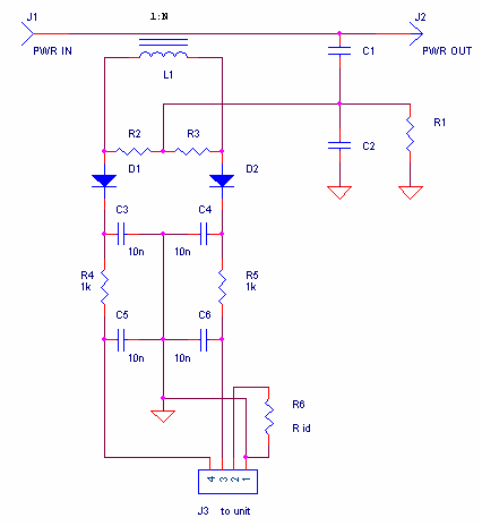
SWR Mega probe

The article should help you to select correct values for component used, based on power and frequency range.



Short theory

The circuit is in fact just 3 voltage sources.

- U1 = voltage divider created by C1 and C2, the resulting voltage is proportional to HF voltage.
- U2 = current transformer loaded by R2, the resulting voltage is proportional to HF current and in case of non reactive load is in phase with U1 signal.
- U3 = current transformer loaded by R3, the resulting voltage is proportional to HF current and in case of non reactive load is in opposite phase with U1 signal.

In situation when the load is non reactive (just resistance, voltage and current in phase) and equal to Zo all 3 voltages have the same amplitude.
The detectors are wired in way that forward signal is U1 + U2 (diode D1) and reverse signal is U1 + U3 (diode D2). So in situation the load impedance is Zo the forward RF voltage signal is double value of U1 (or U2, no difference) and reverse RF voltage is zero.
Detectors work as peak detector, so the rectified DC voltage is RF voltage * 1.4142. But there is also a small voltage drop across the rectifier because of its characteristics (we can ignore that for now).

Lower frequency limit

There are 2 circuits that limit the frequency range from bottom. One is current transformer. Because the secondary winding has finite inductivity and it is loaded by non zero resistor (you can imagine the current source feeds parallel combination of load resistor (R1+R2) and inductance of winding) the first limit freq is
f1 = (R2 + R3) / (2 * Pi * L) [Hz, H, Ohm]
The other limit is set by voltage divider. Because of resistor R1 the voltage starts dropping when is freq goes bellow (we ignore C1 which is much smaller than C2)
f2 = 1 / (R1 * C2 * 2 * Pi) [Hz, Ohm, F]

If we are lucky enough and we construct the meter in way f1 is equal to f2, we can still have the voltage drop but because both voltages drop in the same way (and, more important the voltage phase changes in same way) the calculated SWR value should be still true, also bellow the frequency limit.

Higher frequency limit

Is done by parasitic parameters of components and design itself.
One is capacitance of L1 transformer winding: some current doesn't go to resistors but is closed in that capacity. It reduces sensitivity. Make the winding one layer only, keep the ends apart.
Next one is the loss in core – check maximum usable freq given by manufacturer.
The last one is inductance of R1 and R2. Because both resistors have low ohmic values the small inductance can give significant error. So it is important to use high quality resistors (definitely avoid use of wire type resistor).
The capacitor C2 has to keep its capacity in all frequency range. Parasitic inductance can decrease the voltage (in catastrophic case both create serial resonance – we must always be far bellow that point!). Solution – keep the leads of C2 short as possible and better use several smaller capacitors in parallel to lower that danger.
Unfortunately to compensate the higher freq limit is much harder than the lower one, the amateurs can be happy when they construct the probe with range 1 to 30 MHz, sufficient of short wave station.

Diode bias

Consider a DC current loop for both detectors. There is one common point – resistor R1 (in fact R2 and R3 are engaged too, but they have neglectable low resistance). The current coming through this resistor is sum of currents flowing to both indicator loads. Where is the problem? Let suppose we have low resistance indicator for forward signal. The current of forward signal creates significantly high voltage across R1. This voltage creates also reverse bias voltage for reverse signal detector! As result the reverse detector becomes less sensitive, resulting in lower reverse DC signal / better SWR shown than the real value is! Of course, when the indicator load is significantly higher than R1 that voltage is neglectable (let say, if the SWR mega load is around 1 MOhm and R1 around 1 kOhm, the voltage drop across R1 / bias is about 5 mV, that can be neglected). Of course when the meter load goes to 10 kOhm range (it can happen if you use two classic analog meters, often cross needle meter) that effect can significantly "improve" the SWR indicated.
How to get rid of it completely? Redesign the circuitry in way there is no common resistive component in DC way (there are lots of SWR probe designs). A choke parallel with R1 with much lower resistance can help, too, but be careful, the inductance must be safe high enough not to influence the voltage divider (worst case is the choke and C2 create a parallel LC circuit on measured freq, the divider is giving nearly full RF voltage applied!).

Entry parameters

Rated power Pout – HF power passed that generates required forward DC voltage (in situation when SWR = 1)
Rated HF signal Ur – the voltage equal to values of U1, U2 or U3 in case of matched load (Z=Zo). For SWR Mega and ideal detector Ur = 1.768V (5V / 2 voltage sources /SQRT(2))

Minimum frequency – the frequency where the sensitivity of SWR probe decreases by 3 dB (the power indicated in half of that applied).

Current transformer design

We have a possibility for experiments – we can change the resistor value and number of turns. Because we need given voltage across the resistor by rated power both are tight together by formula

R2/N = Ur/Iout where Iout = SQRT(Pout/Zo).

Example:
Pout = 500W Zo = 50 ohm -> Iout = 3.16A

R2/N = 0.56 ohm/turn.

Say we have nice 10 ohm resistor, then the N = 18 turns.

What power is burned on the resistor?
P = Pout * R2 / (Zo * N * N)

In our case we burn 0.31W, so 1W type should survive.

The R3 is always the same value as R2.

Minimum frequency
We have available toroid core with certain Al constant. The inductance L1 is
L1 = Al * N * N [nH, nH/turn2]

Example:
Al = 50 nH/turn2, 18 turns -> L = 16.2 microH

Lower freq limit f1 = (R2 + R3) / (2 * Pi * L) = 200 kHz

It is deep enough from point of view of HF.

Voltage divider design

The rated power generates output voltage Uout = SQRT (Pout * Zo)
In out case Uout = 158V

The voltage across R2 is
U2 = Iout / N * R2 = 1.757V (should be the same as Ur, but small difference is possible because the number of turns is always a whole number).

So the voltage divider factor is Uout/U2 = 90.

In fact it can be calculated by formula n = N * Zo / R2

Capacitance divider works in way n = C1 / (C1 +C2), we can simplify it also because C1 << C2 to n = C1 / C2.

The capacitor C1 must be robust sufficiently to survive the HF voltage across the line. I make it from part of coax cable, see later.

Let say we make C1 = 3 pF, so the C2 = 270 pF. I suggest to build C2 from several capacitors in parallel, let say 3x 68 pF, 1x 47 pF plus trimmer 50 pF to compensate component tolerances.

Just for information – the current based on our example by max. freq 30 MHz is 90 mA!

The resistor R1 can be calculated based on assumption f1 = f2
R1 = 1 / (2 * Pi * f1 * C2) = 2950 ohm.

In point of view of DC bias (see above) it is better to use lower R1 values; it can increase f2, but it is still acceptable if it is still far enough. Of course, R1 value is not very critical.

DONE!!! All important parts calculated.

73 de Pavel OK1DX January 18, 2010